REMARKS

Claims 1-10 were examined in the April 20, 2007 Office Action. Claims 1-10 stand rejected as anticipated by Applicant's admitted prior art, FIG. 1. Claims 1-10 remain pending, with claim 1 amended above. Reconsideration of the rejection is requested in view of the above amendments and remarks which follow.

A. Anticipation Rejection of Claims 1-10 over FIG. 1 is Addressed.

The rejection of claims 1-10 under 35 U.S.C. § 102(a) as anticipated by applicant's admitted prior art (FIG. 1) is respectfully traversed.

The Examiner's rejection is based on an identification of T10, T7 of FIG. 1 as an inverter. This characterization of two transistors as an "inverter" is incorrect. The circuit T10, T7 is not an "inverter" but rather two transistors having one output node in common. A fairer characterization of the T10, T7 circuit, if one chooses to look at that circuit in isolation, is that it is (i) a PMOS transistor having a first input, a source hard-wired to VLCD, and a drain coupled to the OUT node, and (ii) an NMOS transistor having a second input not coupled to the first input, a source hard-wired to VSS, and a drain coupled to the OUT node. These elements do not collectively constitute an inverter.

It is undisputed that a rejection under 35 U.S.C. § 102(a) must include all the limitations of the claim, including interrelationships between the claimed elements. This is not the case with regard to FIG. 1 and claims 1 and 6. Claims 1 and 6 are deemed to be patentable over FIG. 1 because the "power terminals" of "inverter" T10, T7 are simply not coupled to any "switches", which is required for T10, T7 to constitute an inverter.

Indeed, there are simply no nodes in "inverter" T10, T7 available to be coupled to any switches. The proposed node identified by the Examiner is not available because any circuitry coupled to that node is dead shorted to the OUT node. Furthermore, and bearing in mind that Applicant does not accept the Examiner's characterization of T10, T7 as constituting "an inverter", but must parse out the connections of the T10, T7 circuit based on the Examiner's characterization in order to most clearly distinguish over FIG. 1., the "power terminals" of "inverter" T10, T7 would have to be the source of PMOS transistor and the source of NMOS transistor T7. As pointed out previously, the source of T10 is hard wired to VLCD

and the source of T7 is hard wired to VSS. Accordingly, there are no "switches" as in the present invention. The identified "switching" circuitry is of no use in the Examiner's characterization of the admitted prior art, because it is shorted to the OUT node.

While claims 1-10 are deemed to be allowable as written, in a spirit of cooperation and in an attempt to remove any ambiguities in this matter, claim 1 has been amended to claim "switches" coupled to "power terminals" similar to claim 6. Claim 6 has not been amended as it already contains the "switch" and "power terminals" wording.

Claims 1 and 6 are therefore deemed to be allowable over admitted prior art FIG. 1, since all of the claimed limitations are not taught, even accepting the Examiner's characterization. Remaining claims 2-5 and 7-10 are deemed to be allowable as being dependent upon an allowable base claim. Reconsideration and withdrawal of the § 102 rejection are therefore respectfully requested.

B. Conclusion.

Pending claims 1-10 all being in form for allowance, such action is respectfully requested. Should any issues remain, the Examiner is kindly asked to telephone the undersigned. Although no fee is believed to be due, please charge Deposit Account No. 50-1123 any required fees associated with this filing.

Respectfully submitted,

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